REMARKS

Claims 1-8 and 10-23 remain pending in the application.

The Applicants respectfully request the Examiner to reconsider earlier rejections in light of the following remarks. No new issues are raised nor is further search required as a result of the changes made herein. Entry of the Amendment is respectfully requested.

35 USC 112 First Paragraph Rejection of Claims 1-8, 10-16, 20, 21 and 23

The Office Action rejected claims 1-8, 10-16, 20, 21 and 23 as allegedly containing subject matter which is not described in the specification under 35 USC 112. In particular, the language in claims 1, 7, 13, 20 and 23, i.e., a second agent lacking a dedicated clock, is alleged to lack support in the specification.

The Examiner alleges that the passage cited by the Applicants in the previous response, i.e., page 9, lines 10-14, states that the clock signal may be used as a general processor clock in place of an external crystal oscillator. The Examiner alleges that this does not mean that the agent lacks a dedicated clock, but the clock signal received by the second agent provides the second agent with an internal dedicated clock (Office Action, page 2). The received clock signal allegedly functions dedicatedly internally to the second agent and thus is a dedicated clock (Office Action, page 2). The Applicants respectfully disagree.

Page 9, lines 10-14 recite "The non-super agents which receive the clock signal from the super agent are free to use the clock signal for other purposes as well as for accessing the shared synchronous memory. For instance, the clock signal may be used as a general processor clock in place of an external crystal oscillator."

Applicants disclose that the recited second agent, e.g., a non-super agent, lacks a dedicated clock, e.g., the non-super agent receives a clock signal from a super agent **in place of** an external crystal oscillator.

The Examiner admits the second agent receives a clock, but alleges this received clock provides the second agent with an internal dedicated

clock, functioning internally to the second agent as a dedicated clock (Office Action, page 2).

The second agent receives a clock from **another agent**. The clock **can not** be dedicated if it is shared by two agents. Dedicated is a term of art. A second agent, e.g., a non-super agent, lacks a dedicated clock if it receives its **clock signal from a super agent** in place of an external crystal oscillator.

The Applicants respectfully request the rejection of claims 1-8, 10-16, 20, 21 and 23 under 35 USC 112 be withdrawn.

Claims 17-19 and 22 over Persaud

In the Office Action, claims 17-19 and 22 were rejected under 35 U.S.C. §102(b) as allegedly being anticipated be Persaud et al., UK Patent Application No. GB2074762 ("Persaud"). Applicants respectfully traverse the rejection.

Claims 17-19 and 22 recite, *inter alia*, accessing a portion of an external non-dedicated shared memory from a second agent based on a representation of a single memory access clock signal received **from a first agent**.

Persaud appears to disclose a system and method for accessing a common memory by a plurality of processors (Persaud, Abstract). A master processor can access its own memory or any of the slave memories (Persaud, Abstract). A continuous 02 clock signal is generated on each card (Persaud, page 3, lines 13-14). The continuous clock 02 signal from the master is distributed over the bus to all of the salve processors, together with the master clock signal (Persaud, page 3, lines 15-17). A synchronizing circuit on each slave processor card operates on the master continuous 02 signal to synchronize a slave local clock generator so that it is in synchronism with a clock generator on the master card (Persaud, page 3, lines 17-19). All of the processors are synchronized to each other despite the fact that there is no distribution of clock 02 clock signal over the bus (Persaud, col. 3, lines 19-22).

Persaud discloses a synchronization circuit on each slave processor card that operates on the master continuous 02 signal to synchronize

a slave **local** 6875 clock generator so that it is in synchronism with the 6875 clock generator on the master card (page 3, lines 14-19). In this way, all of the processors are synchronized to each other, despite the fact that when power is first turned on, the clock generators may be out of synchronism (Persaud, page 3, lines 19-22).

Persaud utilizes processors that are driven by a plurality of separate dedicated clocks, i.e., a continuous 02 clock signal is generated **on each card**, that are normally synchronized, but can become de-synchronized (Persaud, page 2, lines 45-47; page 6, lines 10-11). A synchronization signal, i.e., an oscillator clock from the master, is used to synchronize the **plurality of clocks within the slaves** (page 3, lines 13-14). A master processor is synchronized with the slave processor and accesses a slave processor's dedicated memory based on the synchronization of the **plurality** of clocks within the system. Persaud's **plurality** of memory clock signals are received from local clocks, albeit synchronized, **NOT** from a second agent based on a representation of a **single** memory access clock signal received from a first agent, as recited by claims 17-19 and 22.

Persaud discloses a system and method that synchronizes a master clock with slave clocks. Each slave has its own clock generator, i.e., a **local** 6875 circuit, that is synchronized to a master clock signal by a continuous 02 signal. A **plurality** of clock generators is **NOT** a single memory access clock signal, much less a single memory access clock signal that is received **from a first agent**, as recited by claims 17-19 and 22.

The Examiner alleges Persaud discloses a clock generator on a card with a slave processor that receives a Bus Continuous 02 signal from a master, which is the clock signal referred to in the rejection (Office Action, page 6). The local Continuous 02 signal having a representation of the bus continuous 02 signal (Office Action, page 6).

As the Examiner acknowledges, a clock generator is provided on **each** slave card. The Bus Continuous 02 signal from the master is used to synchronize the clock generator on the slave with the master. The clock signal

produced by the slave is not a representation of the master's clock since the slave generates a cock signal through its **own** clock generator.

The Examiner alleges that Applicants' argument that Persaud's clocks are generated locally has no relevance to recited claims 17-19 and 22 (Office Action, page 6).

Persuad discloses a slave memory access that is based on at least **two clock signals**, i.e., a synchronization signal to a clock generator and a clock signal generated by the clock generator. Accessing a memory based upon a synchronization signal and a clock signal generated by a clock generator (two clock signals) is **NOT** accessing a portion of an external non-dedicated shared memory from a second agent based on a representation of a single memory access clock signal received from a first agent, as recited by claims 17-19 and 22.

A benefit of having a second agent access a shared memory with a **single** clock signal received from a first agent is, e.g., synchronization through simplicity. Applicants' system requires only a **single** memory access clock, with all agents sharing the signal. A **single** memory access clock signal synchronizing all agents' access to a shared memory possibly eliminates wasted clock cycles during a transfer of access from a first agent to a second agent. In contrast, Persaud requires the use of a dedicated clock generator for each agent. Having a **plurality** of clock generators creates the problem of synchronization (as discussed by Persaud, page 3, lines 1-22).

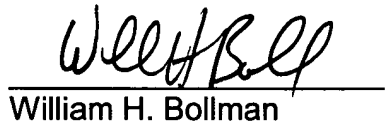
Accordingly, for at least all the above reasons, claims 17-19 and 22 are patentable over the prior art of record. It is therefore respectfully requested that the rejection be withdrawn.

Conclusion

For at least all the above reasons, claims 1-8 and 10-23 are patentable over the prior art of record.

All objections and rejections having been addressed, it is respectfully submitted that the subject application is in condition for allowance and a Notice to that effect is earnestly solicited.

Respectfully submitted,



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